

**APPLICATION  
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**TITLE: ACCURATE WIRE LOAD MODEL**

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## ACCURATE WIRE LOAD MODEL

### Background of Invention

[0001] A typical integrated circuit contains millions of electrical components such as transistors, resistors, capacitors, diodes, and their associated interconnections, which are usually made through conductive materials made of deposited metal, polysilicon, and the like. An integrated circuit's components and their interconnections are typically arranged in a plurality of metal layers which are formed over a substrate typically formed by a silicon wafer. Each layer can contain several thousand conductors. Such conductors are typically electrically insulated from one another by a non-conducting material or dielectric material such as borophosphosilicate glass, silicon dioxide, and the like.

[0002] Figure 1 shows a section of a typical semiconductor wafer (10) having a substrate (12) and a plurality of conductors (14, 16, 18, 20). The conductors (14, 16, 18, 20) are separated from one another and insulated by dielectric material layers (22, 24). The vertical and lateral spacing of the conductors (14, 16, 18, 20) can lead to a phenomenon known as "parasitic capacitance." Capacitance is a natural phenomenon that exists between any two conductors that are not electrically connected to each other; the shorter the distance between two conductors, the larger the capacitance. Parasitic capacitance is termed as such because it is an undesirable effect resulting from the close proximity of conductors in an integrated circuit.

[0003] In Figure 2, exemplary parasitic capacitances are schematically shown as capacitor elements that are joined between the conductors (14, 16, 18, 20), where the conductors (14, 16, 18, 20) are shown for clarity without dielectric material layer boundaries. To calculate, or otherwise determine, the parasitic capacitance attributed to an integrated circuit conductor, the parasitic capacitance can be

broken down into components, as modeled in Figure 2. Particularly, three different components of parasitic capacitance are shown: area capacitance ( $C_a$ ), a coupling or lateral capacitance ( $C_c$ ), and a fringing or fringe capacitance ( $C_f$ ).

[0004] The area capacitance,  $C_a$ , is the component of parasitic capacitance that exists between the top and bottom surface of two overlapping conductors. Accordingly, portions of the top surface of conductor (14) are overlapped by portions of the bottom surface of conductor (16). Hence, parasitic area capacitance can develop therebetween.

[0005] Lateral coupling capacitance,  $C_c$ , is the component of parasitic capacitance that exists between adjacent lateral edges of two conductors. Accordingly, the adjacent lateral edges of conductors (16, 18) can give rise to the shown coupling capacitance.

[0006] Fringe capacitance,  $C_f$ , also known as “edge capacitance,” is the component of parasitic capacitance that exists between a lateral edge of a first conductor and either the top or bottom surface of a second conductor that overlaps, or underlaps, the lateral edge of the first conductor. Accordingly, the leftmost side edge of conductor (16) and the top of conductor (14) can give rise to a fringe capacitance. The fringe capacitance is essentially a distortion to the area capacitance component caused by fringing effects at a conductor’s lateral edges. Similarly, as shown in Figure 2, there are area and fringe components of capacitance between metals and the semiconductor substrate (12).

[0007] An undesirable effect of parasitic capacitance is to slow the propagation of electrical signals through a circuit, thereby reducing the speed at which an integrated circuit can operate. The larger the parasitic capacitance, the greater the delay a signal will encounter as it travels through a conductor. If the components of parasitic capacitance can be extracted from an integrated circuit from the integrated circuit’s physical design, such components can be used to estimate the

delay for signals in the integrated circuit through a process known as “timing and noise analysis.” This information can then be used to adjust the physical layout of the conductors in an integrated circuit, thereby improving the performance of an integrated circuit.

[0008] Typically, within the integrated circuit industry, there are a number of extraction tools, e.g., layout parasitic extractors, that are designed to enable circuit designers to extract and analyze parasitic capacitances. Often, because such parasitic extraction is performed during an early circuit design stage that is prior to the actual layout of the integrated circuit, designers rely on “wire load models” in order to conduct their timing and noise analyses. Thus, due to the earliness of the parasitic extraction stage in the design cycle, the layout of the circuit is typically not yet available, and therefore, designers use general topological structures, such as the one shown in Figure 1, for timing and noise analyses.

[0009] In conventional wire load models, capacitance is a function of wire width, spacing, layer thickness, and interlayer thickness. Such models use general formulas that conform to normal circuit conditions. However, these formulas tend to yield inaccurate findings with reference to real applications because the formulas are formed by consideration of certain layers when certain conditions are true. Further, conventional wire load models may not account for the different kinds of dielectric materials that are used in semiconductor technologies. In other words, previous models are not generic enough for all metal configurations because they are based on relatively simple geometric configurations. Moreover, such models are heavily dependent on technology and have to be redesigned/remodeled as technology changes.

## Summary of Invention

[0010] According to one aspect of the present invention, a method for creating a wire load model comprises creating an interconnect configuration, running a field solver to generate parasitic information for the interconnect configuration, storing the parasitic information in an accessible format, and running a curve-fitting engine to create the wire load model, where running the curve-fitting engine is dependent on the parasitic information.

[0011] According to another aspect, a program storage device readable by a machine that tangibly embodies a program of instructions executable by the machine to perform a method for creating a wire load model comprises creating a wire structure, running a field solver to generate parasitic information for the wire structure, storing the parasitic information in an accessible format, and running a curve-fitting engine to create the wire load model, where running the curve-fitting engine is dependent on the parasitic information.

[0012] According to another aspect, a computer system comprises a memory for storing a model of a circuit, a processor for creating a wire load model (where the processor establishes an interconnect configuration for the circuit), a field solver for determining parasitic information for the interconnect configuration, and a curve-fitting engine that uses the parasitic information to generate the wire load model.

[0013] According to another aspect, a method for creating a wire load model comprises creating an interconnect configuration, generating parasitic information for the interconnect configuration, storing the parasitic information in an accessible format, and creating the wire load model dependent on the parasitic information.

[0014] According to another aspect, a wire load model creation tool comprises means for creating an interconnection configuration for a structure, means for field

solving the interconnect configuration to determine parasitic information, means for storing the parasitic information, curve-fitting means for curve-fitting the parasitic information and using interconnect configuration parameters to create a wire load model, and means for controlling error in the curve-fitting means.

[0015] Other aspects and advantages of the invention will be apparent from the following description and the appended claims.

### **Brief Description of Drawings**

[0016] Figure 1 shows a section of a typical semiconductor wafer.

[0017] Figure 2 shows exemplary parasitic capacitances in a typical semiconductor wafer.

[0018] Figure 3 shows a flow process in accordance with an embodiment of the present invention.

[0019] Figure 4a shows a graphical relationship in accordance with an embodiment of the present invention.

[0020] Figure 4b shows a graphical relationship in accordance with an embodiment of the present invention.

### **Detailed Description**

[0021] Embodiments of the present invention relate to a method for creating an accurate wire load model. Embodiments of the present invention further relate to an apparatus for creating an accurate wire load model. Embodiments of the present invention further relate to a method for generating one or more wire load models that are created differently for different wire structures. Embodiments of the present invention further relate to an apparatus that generates one or more wire load models that are created differently for different wire structures.

Embodiments of the present invention further relate to a method and apparatus for generating one or more wire load models using a curve-fitting engine having an error control mechanism.

[0022] Figure 3 shows an exemplary flow process in accordance with an embodiment of the present invention. Specifically, Figure 3 illustrates flow process by which one or more accurate wire load models may be generated for different interconnect configurations. Initially, structures are created for all possible metal layer combinations (step 30). In this step, sample widths and spacings for the individual metal layers are chosen, where the sample width and spacing of a particular metal layer may be 1, 2, 4, 8, 16, and 32 times a minimum width and spacing specification for that particular metal layer (step 30). Those skilled in the art will appreciate that other embodiments may use a number other than the ones listed above for choosing a sample width and spacing for a particular metal layer.

[0023] For the interconnect configurations created above, a field solver is used to determine parasitic resistance and capacitance numbers, where the numbers are collected in an easily accessible format (step 32) such as a look up table. Those skilled in the art will appreciate that other formats may also be used.

[0024] Then, using the collected information of parasitic resistances and capacitances, a curve-fitting engine, or other similar engine, is used to generate accurate wire load models according to Equations (1)-(4) given below (step 34).

$$C_g = C_a + C_f \quad (1)$$

$$C_f = C_{f0} \times (1 - k_1 \times e^{-k_2 S}) \quad (2)$$

$$C_a = W \times C_{a0} \times \frac{S}{S + S_a} \quad (3)$$

$$C_c = C_{c0} \times (1 + C_{c1} \times \frac{W}{W + W_c}) \times e^{-C_{c2} \times (S - S_0)} \times (\frac{S_0}{S})^{(C_{c2} + C_{c3} \times W)} \quad (4)$$

where  $C_g$  represents ground capacitance,  $C_a$  represents area capacitance,  $C_f$  represents fringe capacitance,  $C_{f0}$  represents a first order value of fringe capacitance,  $k_1$  represents a first coefficient,  $k_2$  represents a second coefficient,  $W$  represents a width,  $C_{a0}$  represents a first order area capacitance,  $S$  represents a spacing,  $S_a$  represents an area capacitance spacing,  $C_{c0}$  represents a first order coupling or lateral capacitance,  $C_{c1}$  represents a second order coupling or lateral capacitance,  $W_c$  represents a lateral capacitance width,  $C_{c2}$  represents a third order coupling or lateral capacitance,  $S_0$  represents a first order spacing, and  $C_{c3}$  represents a fourth order coupling or lateral capacitance. The coefficients used in Equations (1)-(4) are different for different structures. Further, those skilled in the art will appreciate that in other embodiments, similar formulations or derivations of Equations (1)-(4) may be used.

[0025] Those skilled in the art will appreciate that Equations (1)-(4) are so developed as to allow the curve-fitting engine to have error control. In other words, the curve-fitting engine also has an error control mechanism by which an error bound may be specified for a particular curve-fitting. Via Equations (1)-(4), the curve-fitting engine allows one to control error by specifying the amount of error that can be tolerated.

[0026] As stated above, once parasitic information is collected (step 32), a non-linear curve-fitting engine, according to Equations (1)-(4), creates one or more wire load models, where the one or more wire load models are created based on the values used in Equations (1)-(4).

[0027] Those skilled in the art will appreciate that a wire load model library may be created using the wire load model data for interconnect configurations generated by the flow process discussed with reference to Figure 3. One or more such libraries may be then used by circuit simulation engines, noise and timing analysis engines, etc.

[0028] Figure 4a shows an exemplary relationship between ground capacitance and layer width generated by the technique discussed above with reference to Figure 3. Further, Figure 4b shows an exemplary relationship between coupling capacitance and layer width generated by the technique discussed above with reference to Figure 3. Further, Figures 4a and 4b show the relationships with reference to a standard field solver.

[0029] Advantages of the present invention may include one or more of the following. In some embodiments, because a technique to create one or more wire load models uses information specific to individual wire configurations, the one or more wire load models are accurate for all metal layers.

[0030] In some embodiments, because a creation of a wire load model depends on parameters and variables specific to a particular wire structure, the wire load model is flexible in that it can be modified/adjusted for different wire structure conditions.

[0031] In some embodiments, because a creation of a wire load model accounts for dielectric properties affecting a wire, conditions pertaining to various semiconductor technologies may be accounted for in the creation of the wire load model.

[0032] In some embodiments, because a creation of a wire load model accounts for dielectric properties affecting a wire, conditions pertaining to dielectric parameters, e.g., dielectric widths, dielectric constants, etc., may be controlled in the creation of the wire load model.

[0033] In some embodiments, because a creation of a wire load model accounts for a plurality of properties affecting a wire, conditions pertaining to one or metal layers may be accounted for in the creation of the wire load model.

[0034] In some embodiments, because a curve-fitting engine that generates a wire

load model accounts for a plurality of properties affecting a wire, one may account for metal layers above and/or below the wire.

[0035] While the invention has been described with respect to a limited number of embodiments, those skilled in the art, having benefit of this disclosure, will appreciate that other embodiments can be devised which do not depart from the scope of the invention as disclosed herein. Accordingly, the scope of the invention should be limited only by the attached claims.

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